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# Robust approach to verify Training requirements and Performance of HBM


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# Agenda

- HBM overview
- Why HBM training?
- DDR vs HBM
- Verification Environment for HBM IP
- Functional Verification overview
- Types of Training
- Training Verification
- Performance Monitoring
- Summary

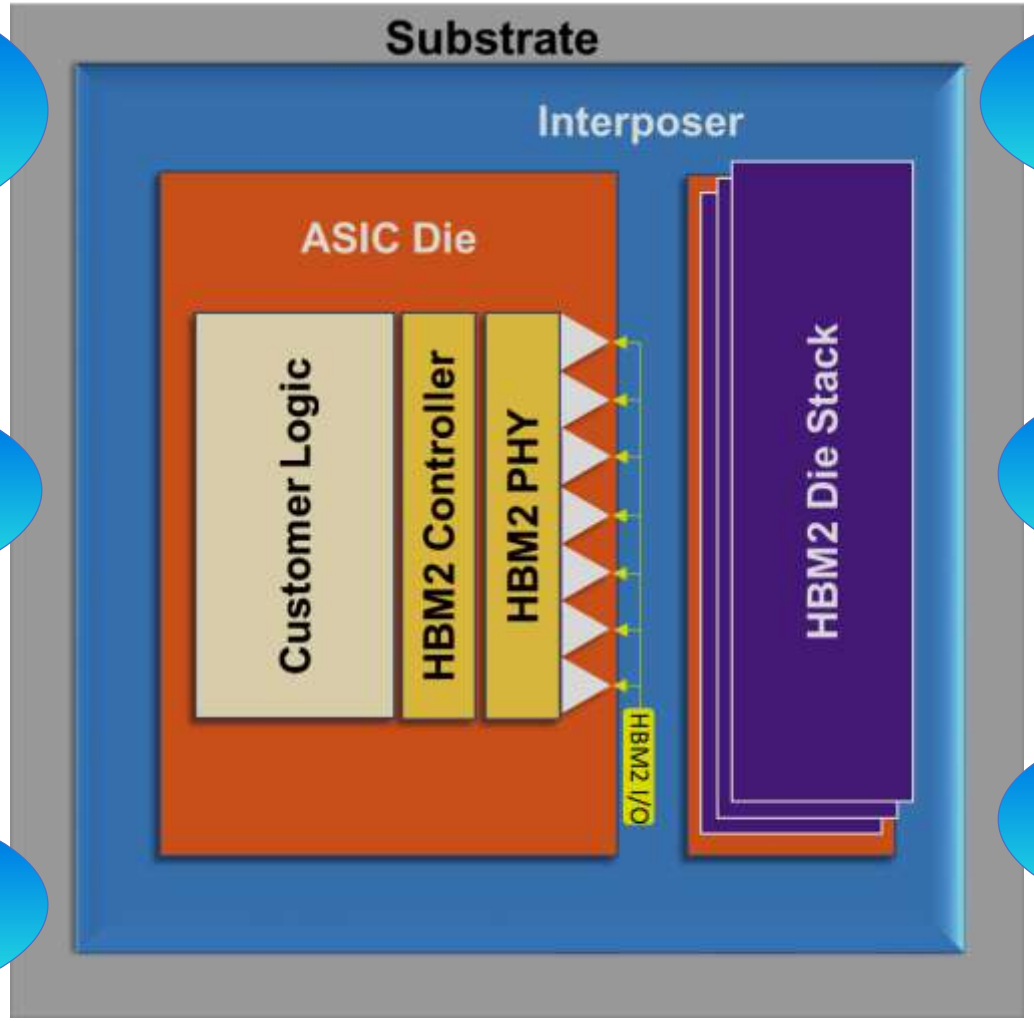
# HBM (High Bandwidth Memory)



High Performance

256 GBps

Shortens information commute




2.5 D tech

3D stacked memory

Low power

# Why HBM training ?

- High frequency operation (1Ghz)
- Variations of Interposer and vendor die
- PVT
- Timing critical
- Package pin faults
- Identify IEEE address mapping between PHY channel and memory die

**Need for smart logic which aligns the link between host and the HBM memory to achieve perfect sampling i.e. Training!**

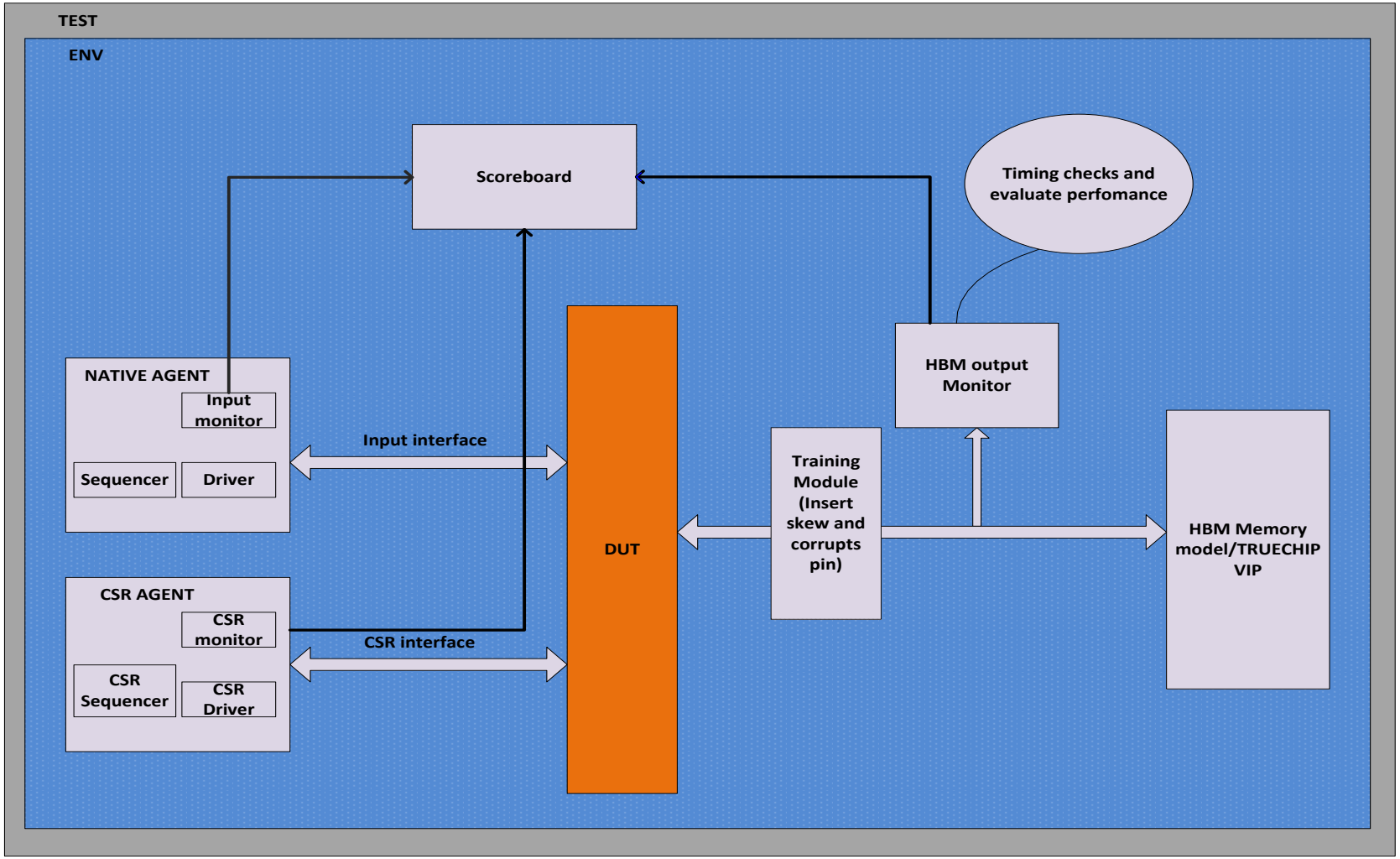
# Training : HBM Vs DDR



Unlike DDR, HBM training supports :

- **Channel Identification**
  - Identification of HBM controller channel connectivity to HBM stack channel
- **AWORD/DWORD remap**
  - Identification of a dysfunctional ADDR or DATA pin and remapping it to a redundant pin
  - Remap instructions used to convey repair information to and from controller
    - Hard lane repair
    - Soft lane repair
- **Channel Level training**
  - DDR : Trained at slice level
  - HBM : Trained at channel level

# Verification Environment for HBM IP



# Verification Environment for HBM IP



Environment Blocks:

- **CSR Driver**
  - Drives configuration signals on CSR interface

- **Native Driver**
  - Drives traffic on native interface as per the protocol

- **Input Interface Monitor:**
  - Monitor activity on native interface and validate protocol
  - Collect the transfers (Data, ID, BA, RA, CA , etc. ) and send to scoreboard

# Verification Environment for HBM IP (…contd)



- **HBM monitor**
  - Monitor activity on HBM interface
  - Validate all timing requirements using assertions
  - Evaluate Memory Controller performance based upon input pattern
- **Dynamic Skew insertion block**
  - Insert skew on HBM pins
  - Static or run-time skew insertion
  - Pin corruption
  - Channel swapping
  - WSO swapping
- **Scoreboard**
  - Confirms data integrity
  - Compare request and response counts

# Testbench Highlights



- UVM based, Directed –Random
- Completely configurable Testbench as per RTL config:
  - **Number of channels supported (1-8)**
  - **Bus widths**
  - **Number of banks**
  - **Latencies**
  - **Feature ON/OFF (DBI,DM,PAR)**
  - **ECC mode**
  - **Frequency ratio**
- Supports both functional and training verification
- Independent frequency controls for all channels with relative skew insertion during training
- Fast Sim option
- Command line switching between various Memory models/VIPs

# Testbench highlights (Functional)



**Functional verification includes :**

- Power Up sequence
- HBM protocol compliance as per JEDEC
- Data integrity
- Error injection and check
  - DERR
  - AERR
  - ECC
- TEMP variations and its effect (Refresh)
- CATTRIP
- Timing checks

# Training types and verification (I)

- Channel Identification
  - Channel swapping
  - WSO swapping
- Remap
  - Pin fault insertion
  - Hard lane repair
  - Soft lane repair
  - DWORD remap : Mode1, Mode2
- Address and Data Training
  - Dynamic skew insertion which results in re-training
  - Complete sweep between skew limits
- Error training
  - AERR and DERR skew insertion

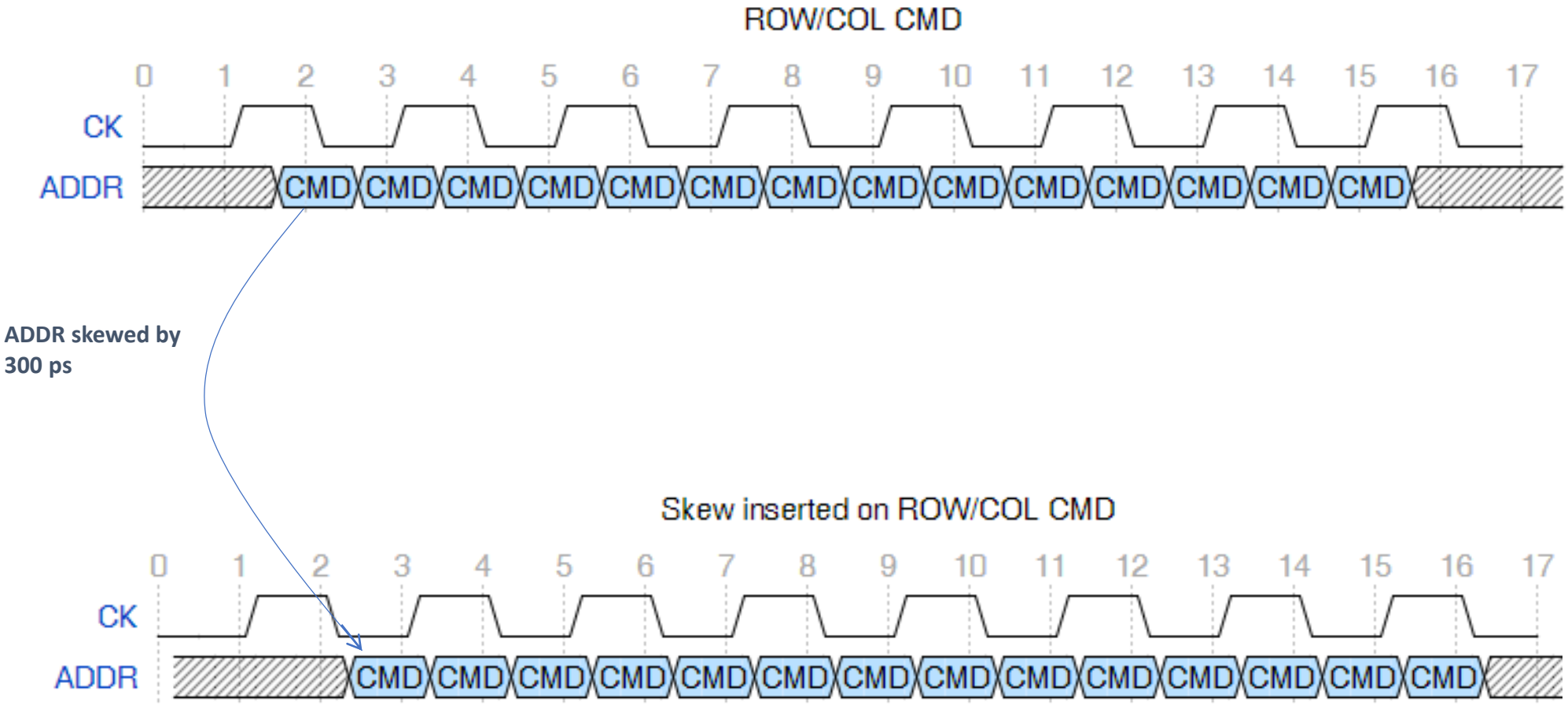
# Training types and verification (II)

- CK-CMD
  - Support to insert skew on CK and command bus for each channel
  - Verify alignment of row and column commands with respect to CK

- CK-WDQS
  - Support to insert skew on CK and WDQS for each channel
  - Verify alignment of WDQS with respect to CK

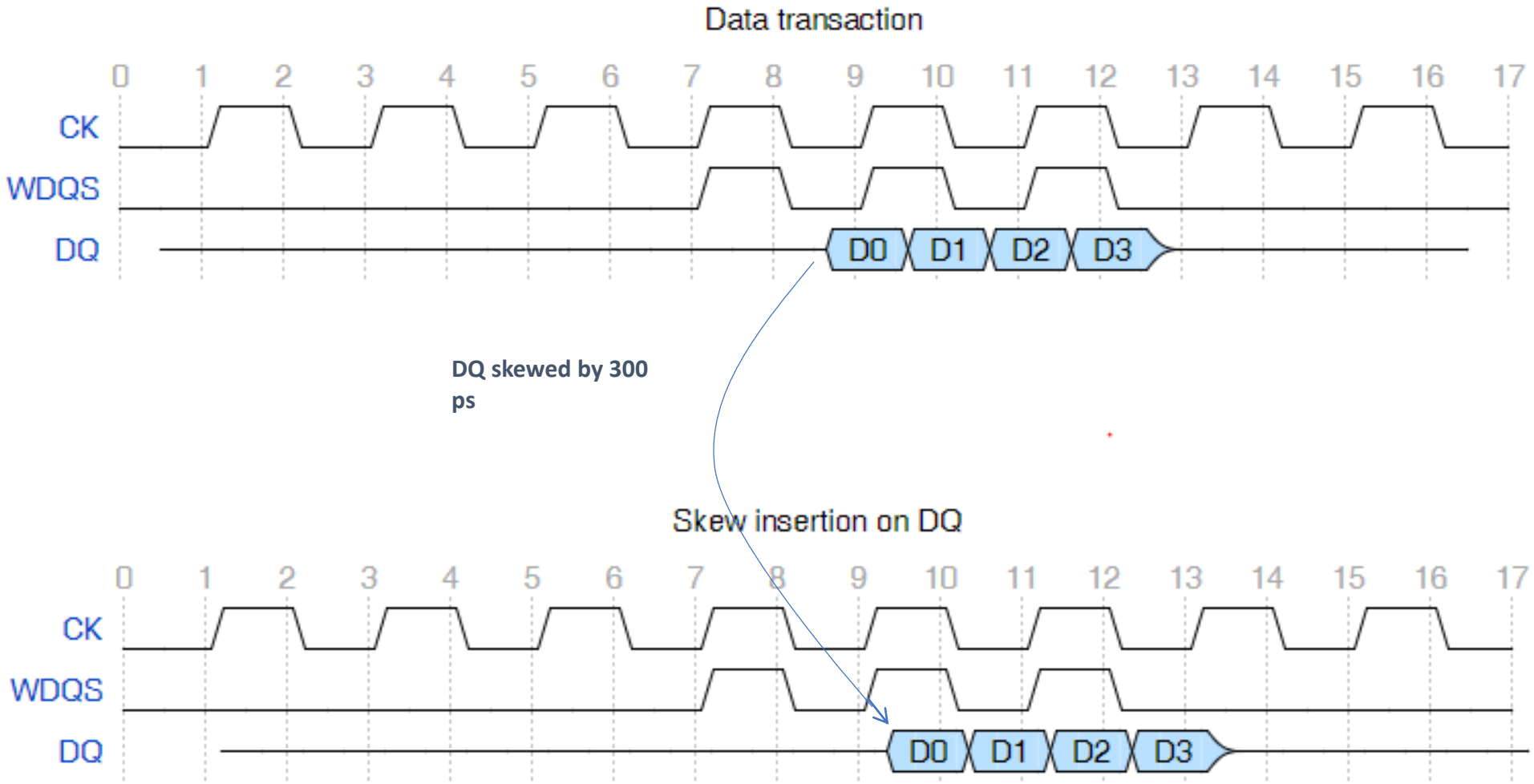
- DQS-DQ
  - Support to insert skew on RDQS/WDQS and DQ for each channel
  - Verify alignment of DQ with respect to RDQS/WDQS

# AWORD skew insertion



# DWORD skew insertion





# Training types and verification (III)

- Configurable support in test bench for group/pin level skew insertion
- Both inter-group and intra-group skew insertion supported
- Test bench is capable of training in User mode using custom register access provided
- Monitors for exact passing window (data eye) comparison for inserted skew

# Performance Monitoring



Testbench capable of monitoring

- Average latency
- Min/Max latency
- In-flight Requests
- Actual Bandwidth
- Expected Bandwidth calculation as per pattern
- Tests cover different traffic patterns for analysing efficiency , for e.g.:
  - RCB/BRC/RBC
  - Only Writes
  - Only Reads
  - Wr-Rd-Wr-Rd

# Summary

- Verification environment provides robust approach to verify training requirements of a high bandwidth memory controller IP
- Verification sign off with zero failures in regression
- 100% code and functional coverage
- Robust verification approach ensured faster silicon bring-up

# Questions?

# Thank You!