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Implications & modus operandi applied for 100% FSM Coverage Closure

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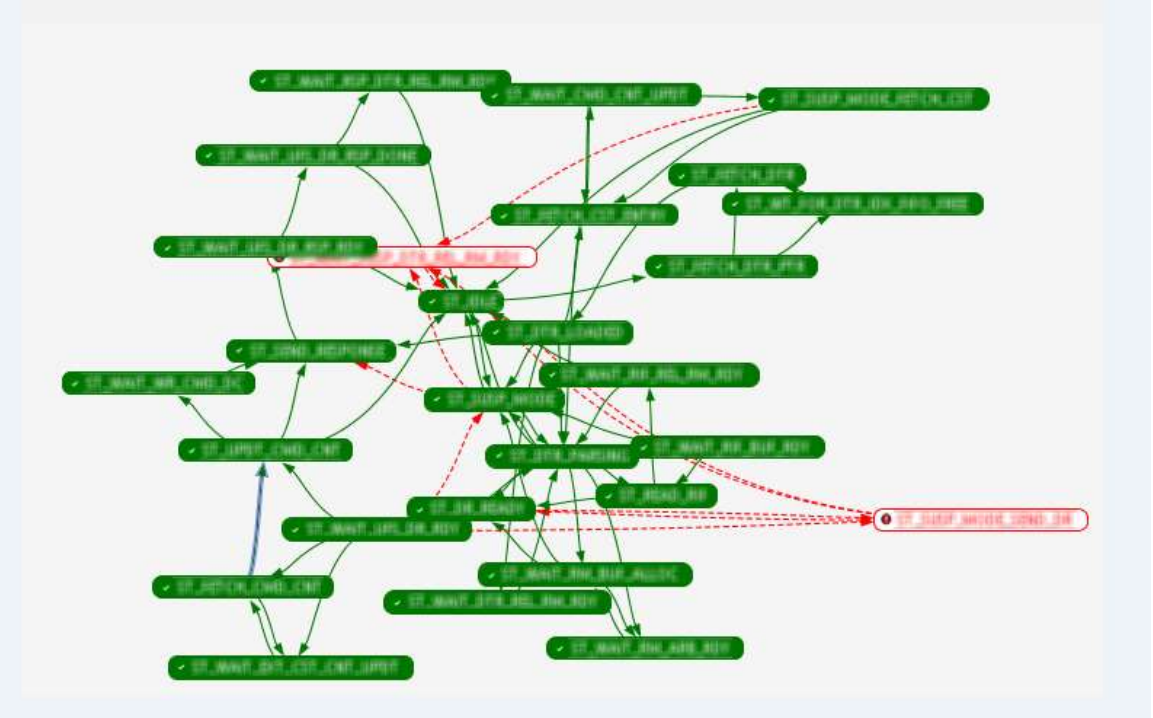
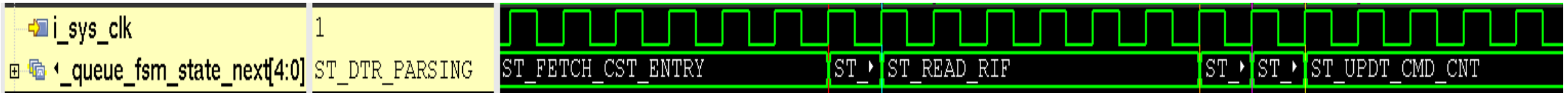
INTRODUCTION

- Finite state machine coverage closure is one of the trivial aspects in the sign off for Design verification closure.
- FSM ensures that all the state transitions have been hit.
- In complex IP designs, getting closure on the FSM is a challenge as certain states requires only one clock cycle for transitioning.

FSM Arc Transition Diagram & WAVEFORM INFERENCE

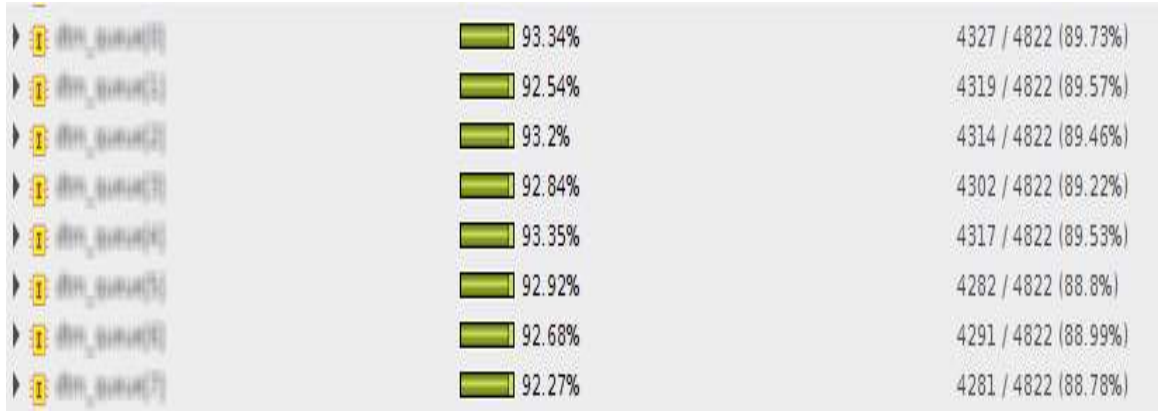
- The red arcs details the uncovered transitions.
- The various colored markers states that there may be transitions with even single clock.





FSM Coverage Status

- The FSM Metrics after the constrained randomization.
- The uncovered transitions after running 5000+ regression runs.



Challenges in Closure

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- Constrained Randomization helps to increase a marginal increase of the Coverage.
- A multi thread forked process to apply stimulus randomly from the tb environment.
- Forcing the hardware signals in the DUT is not an elegant approach.
- So, the predictability of the fsm states and applying the definite stimulus is required.

Approaches Proposed I: Using RAL

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- Using the RAL methodology defined in UVM, we can use the access methods like, register backdoor to capture the fsm states in zero delay time.
- Again using a backdoor write to the registers and applying the stimulus will help us for the fsm transitions hit.
- To use the backdoor access, the hdl path needs to be registered in the top level to access the simulator database hierarchy.
- // Add the ctrl hdl_path starting at bit 0, hardware target is 14 bits wide
- ctrl_reg.add_hdl_path_slice("ctrl", 0, 14);
- //
- // ....
- //
- // Assign DUT to the hdl path
- add_hdl_path("DUT", "RTL");

Approaches Proposed II: XMR Interface

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- In TB, where the packages are imported. The backdoor access are not valid, as we can't use the hierarchical paths. In that case, cross module reference(XMR) of the DUT signals is appreciated.
- By using XMR, we can refer to any object of a module in any other module in either way of upward or downward hierarchical reference.
- repeat(200) begin

```
@(posedge xmr_if.clk) if (xmr_if.q_fsm_state[0]=='d14) begin
$display($time, "The fsm state val is: %h", xmr_if.q_fsm_state[0]);
void'(uvm_hdl_force("ufs_him_top_tb.ufs_card_top.ufs_him.u_ufs_him_DVFS.u_dtm_top.dtm_regs_apb_slave_inst.o_dtm_dtr_queue_suspend_susp_req[7:0]",1));
break;
end
```

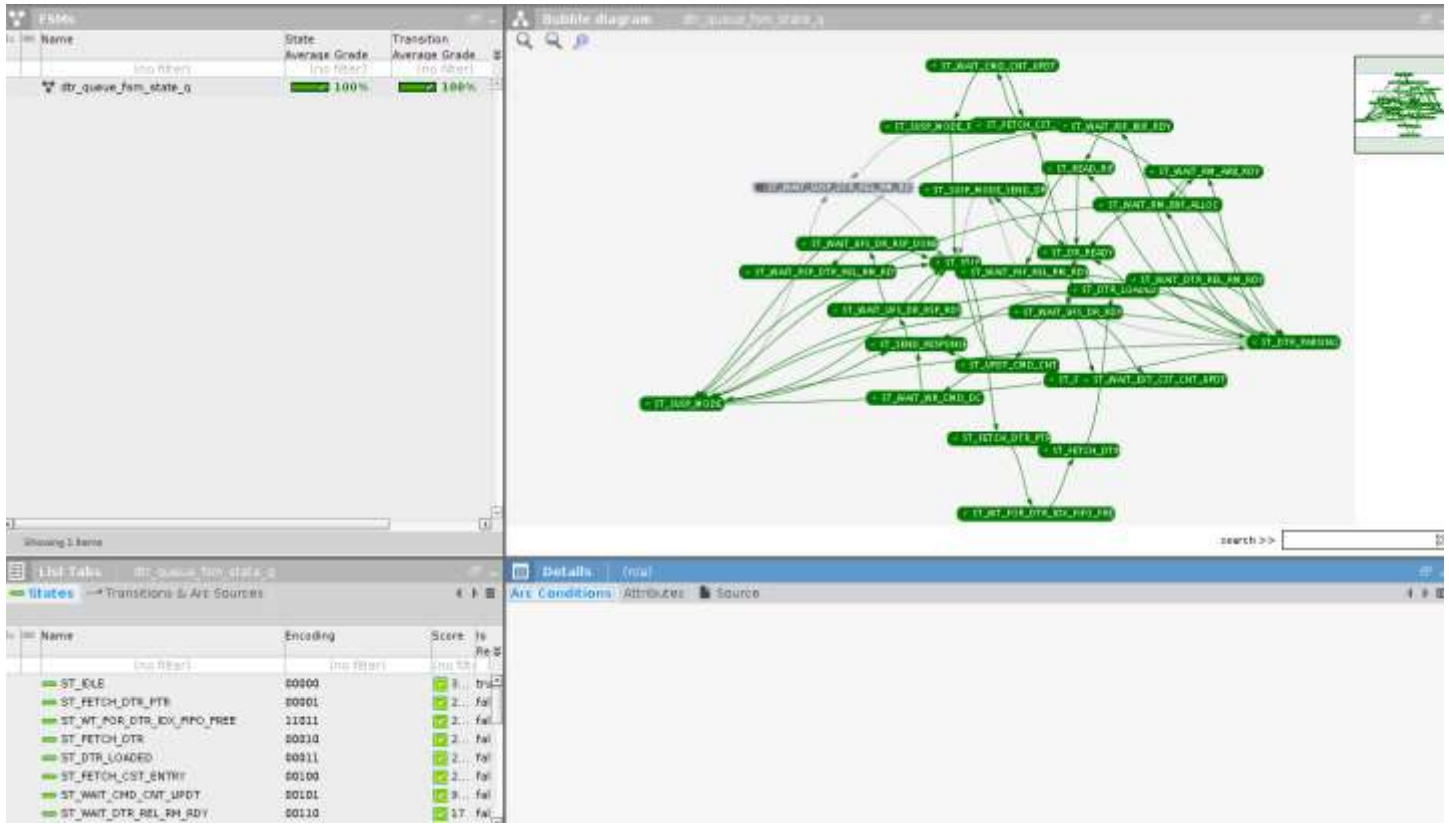
```
void'(uvm_hdl_release("ufs_him_top_tb.ufs_card_top.ufs_him.u_ufs_him_DVFS.u_dtm_top.dtm_regs_apb_slave_inst.o_dtm_dtr_queue_suspend_susp_req[7:0]"))
```

Approach proposed: III

- FSM State scanning Technique.
- This approach is to record the FSM states in testbench/sequence by applying a stimulus.
- Post scanning the states, then sending back the deterministic access and closing on the transitions.

SIMULATION RESULTS

ufs_him_top_tb.xmr_if.clk	1
⊞ ‹_queue_fsm_state_next[4:0]	ST_WAIT_UFS_DR_RDY
⊞ ‹ueue_suspend_susp_req[7:0]	'h 00



RESULTS

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- As a result of these novel methods employed in the FSM closure and the DV sign off,
- 1. We are able to reach up to 100 % FSM Coverage for all the eight instances within three weeks of timeframe.
- 2. A huge effort required has been saved in various aspects.
- a. By time taken for directed tests from the estimate of 2 months to random tests in 2 weeks,
- b. Running multiple regressions of around 5000 count with n number of random seeds to almost 500 count saving 90 % of effort.
- c. EDA tool licenses were effectively optimized for various other activities and reducing the cost of the project.
- 3. Finally, a considerable cost has been saved by alleviating the need for dedicated resource, license and time optimizations.

REFERENCES

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